REMARKS

Claims 1-38 were presented for examination. Of these, the Examiner withdrew claims 27-38 as purportedly being directed to a non-elected invention. Herein, claims 27-38 have been cancelled; claim 1 has been amended; and no new claims have been added. Reconsideration is requested.

After-final amendment entry is proper

Although the amendment to the claims is proposed after a final rejection, entry of this amendment is proper under 37 CFR §1.116. The amendments to claim 1 place all claims in condition for allowance. More specifically, the amendments (1) limit the claim to a controller for power supplies wherein the logic core supplies signals to control said power supplies and (2) specify that the inputs selected for monitoring by the logic core can be varied as the controller changes state. No further searching is required. If the Examiner is not in agreement that these amendments result in allowance, they certainly narrow the issues for appeal.

The amendments to the drawings and specification could not have been made earlier as the Examiner had not previously objected to the drawings or specification. Indeed, the drawings were previously indicated to have been accepted.

The amendments to claim 1 are not required in order to distinguish over Brown. Applicant's previous argument was clear and correct. Brown does not show the operation of the logic core being modified in accordance with data in the memory as the state machine changes state. Thus, it was not predictable that the Examiner would maintain his rejection. In doing so, the Examiner selectively quoted only a part of Applicant's argument, out of context, and failed to take into account why Applicant stated that Brown's collection of state machines do not function collectively as a state machine.*

* That is, contrary to the Office Action, Applicant had both taken this position and supported it with a reason.

Applicant argued that claim 1 requires that the state of operation of the logic core is modified ("upon the transition from a state to a succeeding state") and that in Brown "one sees that its logic is not modified as a result of state transitions." (Emphasis added.)

Election/restriction

Applicant has cancelled, without prejudice or disclaimer, claims 27-38, which had been withdrawn from consideration by the Examiner.

Drawings

In response to the requirement for corrected drawing sheets, Applicant submits herewith replacement sheets for all of Figs. 1-10. In the replacement sheets, the corrections requested by the Examiner have been made. No other changes have been made.

Specification

The Examiner had required a new title. Accordingly, the application has been re-titled "CONTROLLER FOR POWER SUPPLIES." This new title is clearly indicative of the claimed invention.

Claim rejections - 35 U.S.C. §102

Claims 1, 3-5, 7, 10-14, 20-22 and 25-26 have again been rejected under 35 USC §102(e) as purportedly being anticipated by Brown '139. Applicant disagrees, particularly in light of the above amendment, and requests reconsideration.

Amended claim 1 defines a controller for a plurality of power supplies, wherein the controller functions as a state machine and upon the transition from one state to a succeeding state, the operation of the logic core is modified in accordance with data held in the memory, "such that the inputs selected for monitoring can be varied as the controller moves from state to state." Consequently, in some states, an input can be masked off such that it cannot affect the decision-making process. However at other times, an input can be selected for monitoring because its status is important to the decision-making process as it then appears. Brown's CSMs,

as further discussed below, either acting individually or in unison to create a state machine, do not possess this characteristic.

The preamble of claim 1 is also amended to clarify that the single controller may be used to control a plurality of power supplies and the body of the claim is amended to make clear that the logic core outputs are "for supplying signals to control said power supplies."

Brown '139 describes a state machine in which the underlying decision process is fixed, but the data that is used in that decision process can be set by the user. For example, the controllers have three registers for information representing the sequencing of the respective supply for normal powerup, normal shutdown and fault shutdown. See col. 7, lines 28-32.

Regarding operation of the CSM for power-up, Brown states the

> CSM is sensitive to one or more conditions of other state machines as configured by one or more 1 bits in the register STRTEN(n). If there are two or more 1 bits in the register STRTEN(n), then respective conditions must be satisfied. That is, an AND function applies for the respective CSM to enable its controlled power supply.

Col. 7, lines 58-64. Thus, the function executed within the CSM is always an AND operation, and the data supplied to the AND operation for start-up can be masked.

Another register, called the SHDNEN(n) register is provided, whereby

> each 1 bit in these registers identifies a state machine to which a respective CSM is configured to be sensitive for normal shutdown. As for the registers STRTEN(n) as described above, any of the registers SHDNEN(n) can have two or more 1 bits for respective state machines, with an AND function applying for the CSM to power down the respective power supply.

Col. 8, lines 42-49.

Brown's CSMs are also responsive to a fault condition:

> each 1 bit in a one of the registers FLTEN(n) indicates that a CSM for which that register is provided is sensitive to fault messages broadcast by the respective state machine corresponding to that bit position in the register. In this case, each CSM responds to a fault message from any one (or more) of state machines for which it has a 1 bit in the FLTEN(n) register, i.e. an OR function applies.

Col. 9, lines 31-37.

Consequently, there is one AND function implemented within the CSM for start-up, one AND function within the CSM for normal shut-down, and one OR function for fault shutdown. The functions are fixed but the data used by the functions is maskable, set by the data loaded from memory into the shadow registers. See col. 5, lines 60-61.

Further, each CSM within Brown only has a single output - to either enable its supply or to disable the supply.

Brown further discloses that the delays can be associated with specific events. For example, a delay for switching a supply on or a delay before switching a supply off. The individual CSM controllers can act in unison to form a more complex state machine - but the machine has an intrinsic weakness. If a power supply fails to start, then there is no way to time out the start-up time and take remedial action. Similarly, the data in the fault detection register or the shut down register is always the same for all time - even though it would clearly be beneficial to mask off some of the fault detection signals (e.g., a supply under-voltage signal) during periods in which a supply has not been enabled.

Manifestly, Brown does not disclose a controller in which, upon the transition from one state to a succeeding state, the operation of the logic core is modified ... "*such that the inputs selected for monitoring can be varied as the controller changes state.*"

As claim 1 is the only independent claim and all the other rejected claims depend from claim 1, it should now be apparent that this entire rejection should be withdrawn.

Claim rejections - 35 USC §103

Claims 2, 6, 9, 8, 15-19 and 23-24 have been rejected under 35 USC §103(a) as purportedly being unpatentable over Brown '139 in view of MacSorley '427. Applicant disagrees and requests reconsideration for the reasons stated below.

Firstly, this rejection is now moot. By the amendment to claim 1 overcoming the only rejection against claim 1, the rejected claims are all allowable as depending from an allowable independent claim.

Nevertheless, for the sake of completeness, this rejection will be discussed briefly.

Applicant appreciates that the Examiner has cited the factual inquiries required by *Graham v. John Deere Co.* However, the Examiner has not addressed all four points of inquiry required by the Supreme Court. For example, the Examiner has not considered the level of ordinary skill in the art. It is incumbent upon the Examiner to do perform the full analysis, as the Board has made clear in several recent post-KSR cases, commencing with *In re Kalliokulju*, BPAI App. No. 2007-0834 (May 10, 2007).

Brown has been discussed at length above. According to the Office Action, Brown fails to disclose an invert signal for causing an output signal from the input detector to be inverted with respect to the input signal, as required by claim 6. So the Examiner turns to MacSorley and finds that MacSorley teaches an invert signal for causing an output signal from the input detector to be inverted with respect to the input signal, and he then concludes that it would have been obvious for a person of ordinary skill in the art to combine Brown with MacSorley, motivated by protection of the storage by storage protection circuitry and addressing the unreachable portion of storage. Respectfully, MacSorley is an 818-page document relating to a large scale data processing system. It does not relate to a state machine controller. In no way would MacSorley have suggested to a person skilled in the art any modification of Brown, let alone the hypothesized modification. There is no reason to believe that one skilled in the state machine controller art would also be familiar with large scale data processing systems or that such large scale data processing systems would suggest any features of state machine controller design for power supplies to such an individual of ordinary skill in the art. MacSorley is not even

analogous art. It is therefore ineligible for consideration as establishing the state of the art in power supply controller design, and ineligible for combination with Brown. See *In re Clay*.

For the foregoing reasons, the Examiner has not carried his burden of establishing a *prima facie* basis for an obviousness rejection.

Applicant could address each of the independent claims and its rejection but will not do so to avoid unnecessarily burdening the record. Nevertheless, it may be noted that the art of record manifestly does not disclose a sequence detector having a timer to check that a condition has happened for a pre-determined time period, as required in claim 13; and neither does the art of record teach or suggest that the data retrieved from the memory should define the output data for the outputs in the next state so that several outputs can change together, as required by claim 23.

For each and all of the foregoing reasons, the rejection under §103 should be withdrawn.

CONCLUSION

A Notice of Allowance is respectfully requested. The Examiner is requested to call the undersigned at the telephone number listed below if this communication does not place the case in condition for allowance.

If this response is not considered timely filed and if a request for an extension of time is otherwise absent, Applicant hereby requests any necessary extension of time. If there is a fee occasioned by this response, including an extension fee, that is not covered by an enclosed check, please charge any deficiency to Deposit Account No. 23/2825.

Respectfully submitted,

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